WHAT IS CLAIMED IS:

1. A semiconductor testing apparatus wherein an input signal of a test pattern is supplied to a semiconductor device, and an output signal obtained from said semiconductor device is compared with a prescribed expected value to conduct a test, said apparatus comprising:

test pattern memory means adapted for storing test pattern data of the test pattern, managing the test pattern data in accordance with addresses, and outputting the test pattern specified by any address;

test pattern generation means for generating a test pattern signal on the basis of the test pattern outputted from said test pattern memory means; and

control means for controlling said test pattern memory means and said test pattern generation means in such a manner that the test pattern signal based on the test pattern data of a desired address can be generated at a predetermined timing conforming to the set information.

2. The semiconductor testing apparatus according to claim 1, wherein the contents of said set information are changeable in compliance with requirements, and said control means controls the timing of generation of the

test pattern on the basis of the latest changed set information, and varies the cycle period to execute the test pattern of the desired address.

3. The semiconductor testing apparatus according to claim 1, wherein said control means controls the timing of generation of the test pattern in such a manner that the cycle period rate to execute the test pattern of the desired address becomes a cycle period narrower than a predetermined rate.

4. A semiconductor testing method for conducting a test of a semiconductor device by supplying an input signal of a test pattern to said semiconductor device and comparing an output signal therefrom with a prescribed expected value, said method comprising the steps of:

managing and storing, in accordance with addresses, test pattern data of the test pattern generated previously;

outputting the test pattern of a desired address at a predetermined timing that conforms with the set information; and

generating a test pattern signal on the basis of the test pattern data of the desired address outputted at said predetermined timing.

5. The semiconductor testing method according to

claim 4, further comprising the steps of:

supplying the input signal of the test pattern to said semiconductor device after variably setting the desired address and the predetermined timing; and

detecting whether any failure has been caused or not in said semiconductor device, thereby analyzing the internal fault in said semiconductor device.